PVP 14

Code: EC5T3

III B.Tech - I Semester – Regular/Supplementary Examinations
MARCH - 2021

COMPUTER ARCHITECTURE AND ORGANIZATION
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) What is the function of Program Counter?
b) Explain memory transfer.
c) Abbreviate and brief RISC.
d) What is an Instruction Format?
e) What is CMOS cell?
f) Explain Parity bit.
g) Write the principle of Booth multiplication.
h) Draw SISD computer system.
i) Define Sequential Execution.
j) Define Data Hazard.
k) State the advantages of data transfer using DMA.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Explain Register Transfer with an example. 8 M

   b) How will you use logic micro operations in Selective set operation and in Selective clear operation? 8 M

3. a) List out the steps that the control must undergo in address sequencing during the execution of a single computer instruction. 8 M

   b) If the stack is FULL =0, how the PUSH operation will work? Explain. 8 M

4. a) Draw the block diagram of Associative Memory. 8 M

   b) Explain various modes of Transfer techniques in computer organization. 8 M

5. a) Explain about Sequential Version of the Multiplication Algorithm and Hardware. 8 M

   b) Provide Floating point Addition and Subtraction flow chart for $Z \leftarrow -X + Y$ *and* $Z \leftarrow -X - Y$ 8 M

6. a) List out and explain the stages of pipelining with a neat diagram. 8 M

b) What is vector processing and also provide vector instruction format? 8 M